EC662

~~Sixth~~ Semester B.E. Degree Examination, June / July 08

DSP Architecture

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1. a. Explain about decimation. Briefly explain how the decimated sequence is obtained. **(06 Marks)**
   b. The sequence x(n) = {0, 4, 8, 12, 16} is interpolated using interpolation sequence $b_k = \{1/4, 2/4, 3/4, 1, 3/4, 2/4, 1/4\}$ and the interpolation factor is 4. Find the interpolated sequence y(m). **(10 Marks)**
   c. Write a MATLAB program to compute linear convolution of the following two sequences. x(n) = {2, 1, -2, 2} and h(n) = {3, 1, 2, -1}. **(04 Marks)**
2. a. Draw and explain the 3× 3 Braun multiplier structure. What is the total propagation delay if each adder introduces 1.5 unit delay? **(10 Marks)**
   b. Identify the addressing modes of the operands in each of the following instructions and their operations. i) ADD B ii) ADD # 2233h iii) ADD 2233h iv) ADD* addrreg, offsetreg + **(05 Marks)**
   c. A sum of 512 products are to be summed up in a MAC using pipelined operation. The inputs to the Mac are 16-bit numbers. The MAC execution time is 50ns. Find i) What will be the total time required to complete the operation? ii) How many guard bits should be provided for the accumulator to prevent the overflow condition? **(05 Marks)**
3. a. Briefly explain the special addressing modes. **(08 Marks)**
   b. Draw the block diagram of parallel implementation of an 8-tap FIR filter using two MAC units and compare it with pipelined implementation. **(06 Marks)**
   c. With the help of functional diagram, explain about the Multiplier / Adder unit of TMS320C54XX processors. **(06 Marks)**
4. a. Describe the operation of the following instructions of TMS 320C54XX processors. i) MPY # 2314, A ii) MAC * AR5- , * AR6+, A, B **(03 Marks)**
   b. Explain what is accomplished by the following instruction sequence. RPT # 3 ; MAC * AR3 - , * AR2+, A **(03 Marks)**
   c. Write TMS320C54XX program to compute the sum of three product terms given by the equation. y(n) = h(0) x(n) + h(1) x(n-1) + h(2) x(n-2), using direct addressing mode. Where h(0), h(1) and h(2) are stored in data memory locations starting at location h and x(n), x(n-1) and x(n-2) are stored in data memory locations starting at location x. y(n) is saved in data memory locations y (low 16 bits) and y+1 (high 16 bits). **(09 Marks)**
   d. Assume that the register AR4 with contents 2040h is selected as the pointer for the circular buffer. Let BK = 50 h. Determine start and end addresses for the buffer. What will be the contents of the register AR4 after the execution of the instruction? i) LD*AR4 + 0%, A ; ii) *AR4 – OB , if the contents of AR0 is 0035h? **(05 Marks)**
5. a. What values are represented by the 16-bit fixed point number N = 5736h in Q0, Q6, Q10 and Q15 notations. **(10 Marks)**
   b. Explain how the IIR filter can be implemented using TMS320C54XX processor (only algorithm is needed). **(10 Marks)**
6. a. Explain how the Bit-reversed index generation can be done in 8 point DIT FFT. **(04 Marks)**
   b. With the help of signal flow graph, explain about the FFT implementation algorithm for 8-point DIT-FFT on the TMS320C54XX . Scale factor for all butterflies = ¼. **(06 Marks)**
   c. Interface an 8k × 16 program ROM to the 'C5416 DSP in the address range 7FE000h – 7FFFFFh. **(10 Marks)**
7. a. Explain the Multi channel buffered serial port (M_C BSP) with the help of block diagram. **(10 Marks)**
   b. Draw the block diagram of the PCM3002 CODEC and explain about it. **(10 Marks)**
8. a. With the help of block diagram, explain the memory interface for TMS320C5416 processor. Also draw the timing diagram for a read-read- write sequence of operations. **(10 Marks)**
   b. With the help of block diagram, explain the Image compression and Reconstruction using JPEG encoder and decoder. **(10 Marks)**

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EC662

~~Sixth~~ Semester B.E. Degree Examination, Dec 08 / Jan 09

DSP Architecture

Time: 3 hrs. Max. Marks:100

Note : *Answer any FIVE full questions.*

1 a. Discuss the basic features to be provided in a DSP Architecture to implement the convolution $y(n) = \sum_{i=0}^{N-1} h(i)x(n-i)$. (08 Marks)

b. Explain with examples the process of Decimation and Interpolation by factor of 2 and 3. (06 Marks)

c. Draw and explain Braun Multiplier Structure to multiply two 4 bit unsigned numbers A and B. (06 Marks)

2 a. Discuss the features of the address generation unit of a programmable DSP. Write a neat block diagram. (06 Marks)

b. Discuss the features of the program sequencer unit of a programmable DSP. Write a neat block diagram. (06 Marks)

c. Describe the implementation of 8 TAP FIR Filter with two MAC units and Eight MAC units. (08 Marks)

3 a. Describe the central processing unit of TMS 320C54 DSP with a neat block diagram. (06 Marks)

b. Discuss any four addressing modes of TMS 320C54 DSP with examples. (06 Marks)

c. Describe the operation of the following instructions :

i) MPY * AR_3 - , * AR_4 + 0, B
ii) MAC *AR_2 + , * AR_3 - , B, A
iii) ADD *AR_2 + , 6, A
iv) ADD # 2345h, - 4, B, A (08 Marks)

4 a. Discuss various categories of programming instructions of TMS 320C54 DSP with atleast one example each. (06 Marks)

b. Write a program to implement using the DSP $A = \frac{1}{16} \sum_{i=0210h}^{021Fh} dmad(i)$. (08 Marks)

c. Implement y(n) = h(0)x(n) + h(1)x(n-1) + h(2)x(n-2), using TMS DSP instruction using MAC. (06 Marks)

5 a. Explain Q notation used in DSP algorithm implementation. What are the values represented by 16 BIT number N = 3000h in Q12 and Q15 notation? (06 Marks)

b. What is an Adaptive Filter? Explain briefly how an adaptive filter can be implemented using DSP. (08 Marks)

c. Explain a PID controller with equations and implementation block diagram. (06 Marks)

6 a. What is the minimum size of FFT of RADIX – 2 that must be used to compute 200 point DFT. Determine the number of butterfly structures, number of complex multiply and additions needed in the FFT computation. (08 Marks)

b. Explain the BIT reversal address mechanism and give its implementation scheme using TMS 320C54 DSP. (06 Marks)

c. Explain how overflow is handled with scaling in the computation of DFT. (06 Marks)

7 a. Explain briefly building blocks of PCM 3002 CODEC unit. (06 Marks)

b. Discuss the implementation of a DSP based bio telemetry receiver. (06 Marks)

c. Give a overview of JPEG algorithm with encoding and decoding algorithms. (08 Marks)

8 Write short notes on any four:

a. Multi channel buffered serial port
b. Pipeline operation of TMS 320C54 DSP.
c. Any two on chip peripherals of TMS DSP
d. Paralleling and pipelining mechanisms for high speed DSP operation.
e. Organization of Chip memory
f. Handling of interrupts in TMS 320C54. (20 Marks)

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06EC74

Seventh Semester B.E. Degree Examination, Dec.09-Jan.10
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, choosing atleast TWO questions from each part.***

PART – A

1 a. Explain the decimation and interpolation process, with an example. **(06 Marks)**

b. The sequence x(n) = [0, 3, 6, 9] is interpolated using interpolation sequence bk = [⅓, ⅔, 1, ⅔, ⅓] and the interpolation factor of 3. Find the interpolated sequence y(m). **(06 Marks)**

c. Describe the basic features that should be provided in the DSP architecture to be used to implement the N^{th} order FIR filter,

$$Y(n) = \sum_{i=0}^{N-1} h(i)x(n-i) \; ; \quad n = 0, 1, 2, \ldots\ldots$$

Where x(n) denotes the input sample, y(n) the output sample and h(i) denotes i^{th} filter coefficient. **(08 Marks)**

2 a. Explain Baugh – Wooley multiplier for signed numbers. Show the multiplication operation for 4 × 4 signed multiplication. **(06 Marks)**

b. What is meant by circular addressing mode? Write pointer updating algorithm for the circular addressing mode and show different cases that encounter during the updating process of the pointer. **(06 Marks)**

c. Explain implementation of 8 – tap FIR filter, i) pipelined using eight MAC units and ii) parallel using two MAC units. Draw block diagrams. **(08 Marks)**

3 a. Compare architectural features of TMS320C25 and DSP56000 fixed point digital signal processors. **(06 Marks)**

b. Write an explanatory note on direct addressing mode of TMS320C54XX processors. Give example. **(06 Marks)**

c. Describe the operation of the following instructions of TMS320C54XX processors.
i) MPY * AR2 - , *AR4 + 0, B ii) MAC *AR5 +, #1234h, A
iii) STH A, 1, *AR2 iv) SSBX SXM. **(08 Marks)**

4 a. Explain the following assembler directives of TMS320C54XX processors. **(06 Marks)**
i) . mmregs ii) . global iii) . include 'xx' iv) . data v) . end vi) . bss

b. Describe Host Port interface and explain its signals. **(06 Marks)**

c. Write an assembly language program of TMS320C54XX processors to compute the sum of three product terms given by the equation, $Y(n) = h_0 x(n) + h_1 x(n-1) + h_2 x(n-2)$ with usual notations. Find y(n) for signed 16 bit data samples and 16 bit constants. **(08 Marks)**

PART – B

5 a. Determine the value of each of the following 16-bit numbers represented using the given Q – notations : i) 4400h as a Q0 number ii) 4400h as a Q7 number
iii) 0.3125 as a Q15 number iv) - 0.3125 as a Q15 number. **(06 Marks)**

b. Write an assembly language program for TMS320C54XX processors to multiply two Q15 numbers to produce Q15 number result. **(06 Marks)**

c. What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and polyphase subfilter. **(08 Marks)**

6 a. Determine the following for a 128 – point FFT computation : i) number of stages ii) number of butterflies in each stage iii) number of butterflies needed for the entire computation iv) number of butterflies that need no twiddle factors v) number of butterflies that require real twiddle factors vi) number of butterflies that require complex twiddle factors. **(06 Marks)**

b. Explain, how scaling prevents overflow conditions in the butterfly computation. **(06 Marks)**

c. With the help of implementation structure, explain the FFT algorithm for DIT- FFT computation on TMS 320C54XX processors. Use ¼ as scale factor for all butterflies. **(08 Marks)**

7 a. Design a data memory system with address range 000800h – 000FFFh for a C5416 processor using 2K × 8 SRAM memory chips. **(06 Marks)**

b. Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode. **(06 Marks)**

c. Describe DMA with respect to TMS320C54XX processors. **(08 Marks)**

8 a. Explain PCM3002 CODEC, with the help of a neat block diagram. **(06 Marks)**

b. Explain DSP – based biotelemetry receiver system, with the help of a block schematic diagram. **(06 Marks)**

c. With the help of a block diagram, explain the image compression and reconstruction using JPEG encoder and decoder. **(08 Marks)**

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